Mercury EMI Reducing Spectrum Clock Oscillators

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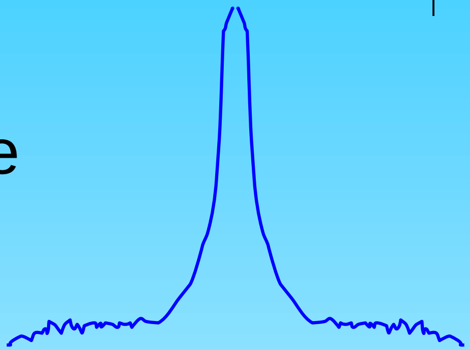
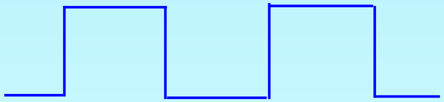
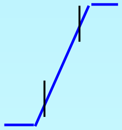
Characteristics of a Conventional Clock

- A perfect clock (high Q crystal) has all its energy concentrated on a single frequency and its harmonics.
  ➔ High Peak Emissions



- 50%-50% duty cycle, faster rise and fall time
  ➔ Higher harmonic energy (unwanted energy) in 3rd, 5th, 7th etc.
  Higher order harmonics have stronger peak energy and emissions





EMI Regulations

- Federal Communication Commission (FCC) part 15

Frequency (MHz)	Radiation (dB uV/m). Class B (3 meters)
30 ~ 88	40.0
88 ~ 216	43.5
216 ~ 960	46.0
Above 960	54.0

Peak Emissions, not average emissions

- International Electrotechnical Commission's International Special Committee on Radio Interference (CISPR) Publication 22 class B limits

Frequency (MHz)	Radiation (dB uV/m), 10 meters
30 ~ 230	30.0
230 ~ 1000	37.0

Peak Emissions, not average emissions

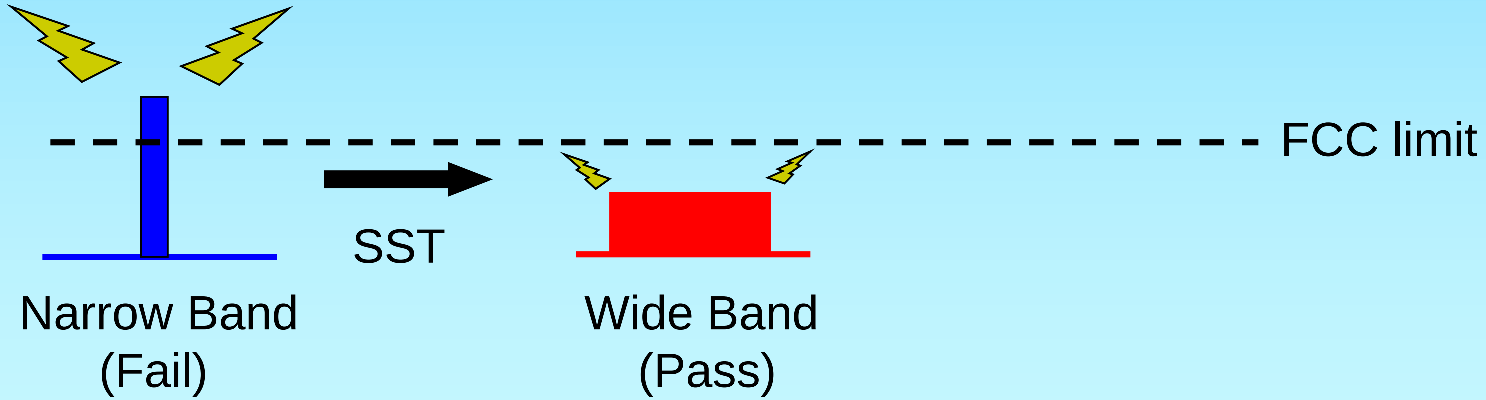
Spread Spectrum Technology

Technique: By slowly frequency modulating the clock frequency between two pre-defined frequency boundaries, radiated emissions are reduced by spreading the emissions over a wider frequency band. Total energy is not changed.

Result: Only a small amount of the total energy is radiated at any particular frequency.

Total energy remains the same

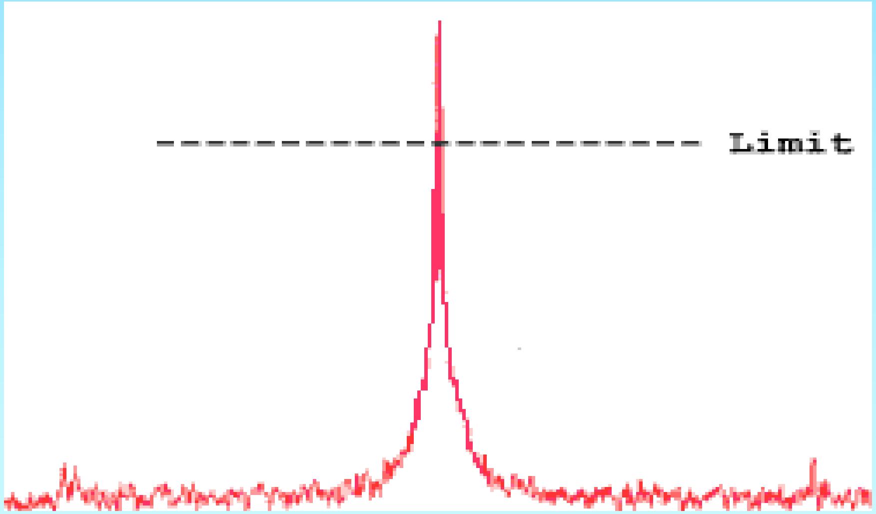
Frequency Modulation → Energy Re-distribution
(Time domain) (Frequency domain)



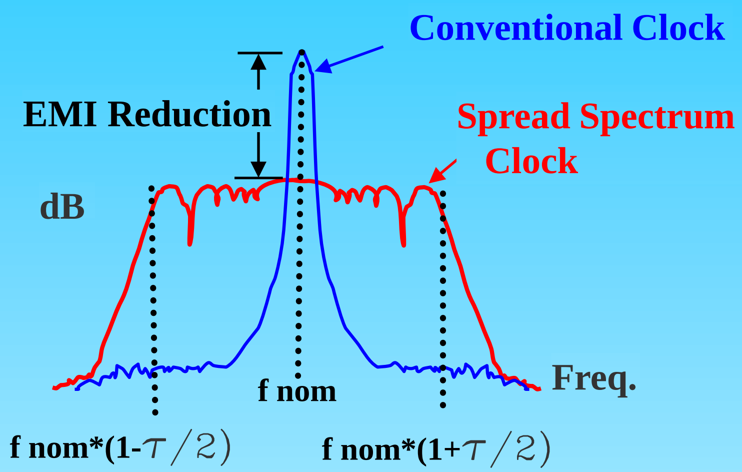
Wider bandwidth→ Wider energy spread→ Greater EMI reduction

Energy Spread Techniques

- Type 1: Center Spread
- Type 2: Down Spread
- Type 3: Down-center Spread
  (asymmetric Spread)

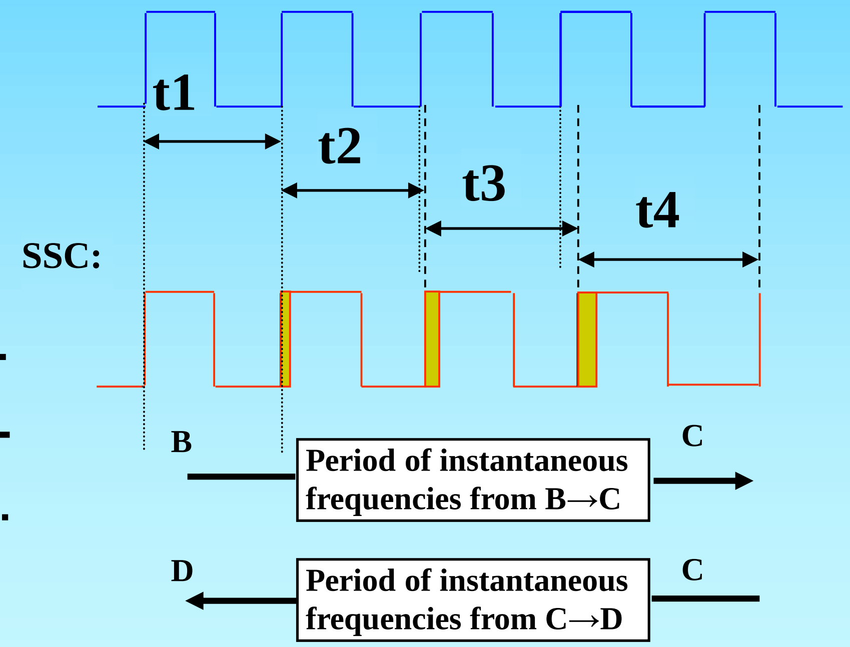


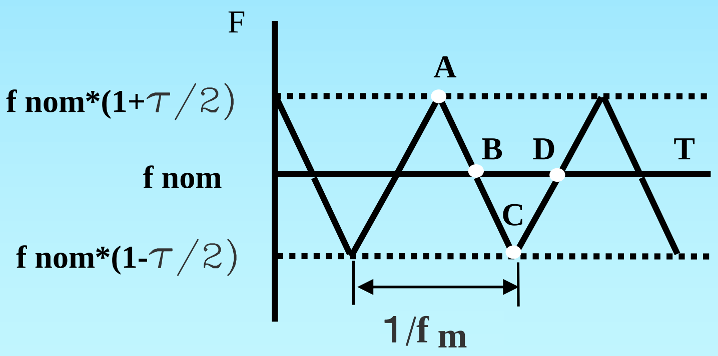
Type 1:
Center Spread: $f_{center} = f_{nominal}$



t1 < t2 < t3 < t4

Periods of instantaneous frequencies:
Conventional Clock at f nom:





"τ ": Total spread %; f m: Modulation carrier frequency

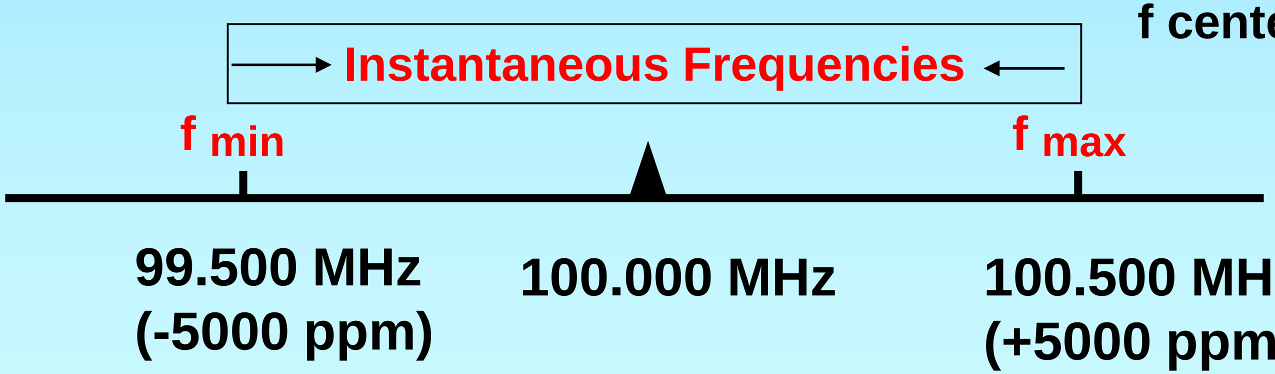
Concerns of Modulation Carrier Frequency

- Must be much lower than the system frequency (KHz range)
- >20 KHz (to be inaudible) to <100 KHz (for PLLs with <10 u sec. tracking)
- Low Impact on jitter, duty cycles, rise and fall time
- Ability of the device receiving the reference to track the variations in frequency

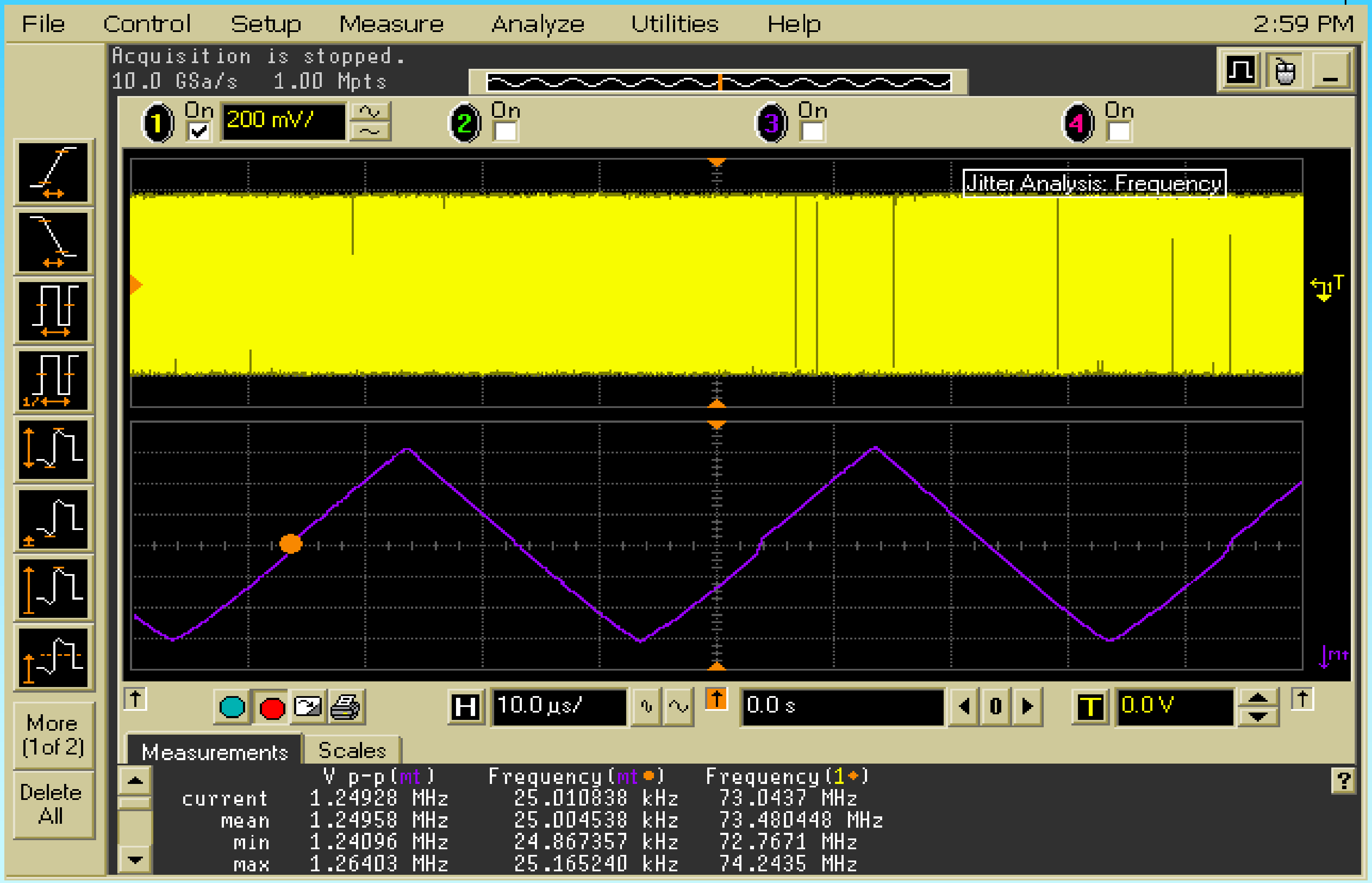
Example:100 MHz with Center Spread at ±0.5% (±5000 ppm)

- $f_{nom.}$=100 MHz = 0.01u sec.
- f_{mod} = 34.688 KHz = 28.82 u sec.
- Cycle Ratio = $\frac{\text{Clock}}{\text{Modulation}} = \frac{\text{2882 cycles}}{\text{1 cycle}}$
- +0.5%: 1441cycles above f nom;
  -0.5%: 1441 cycles below f nom. ($\Delta f_{up} = \Delta f_{down}$)

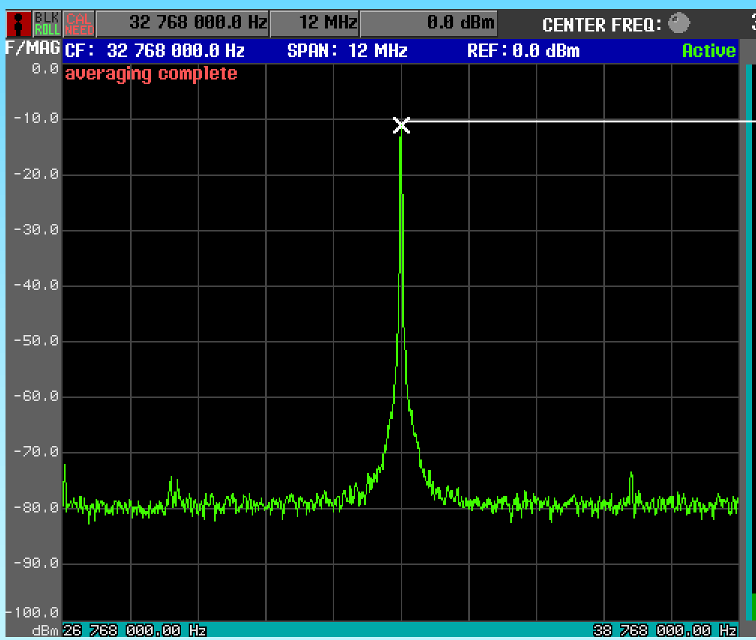
f center = f nominal



Clock Frequency and Modulation Frequency



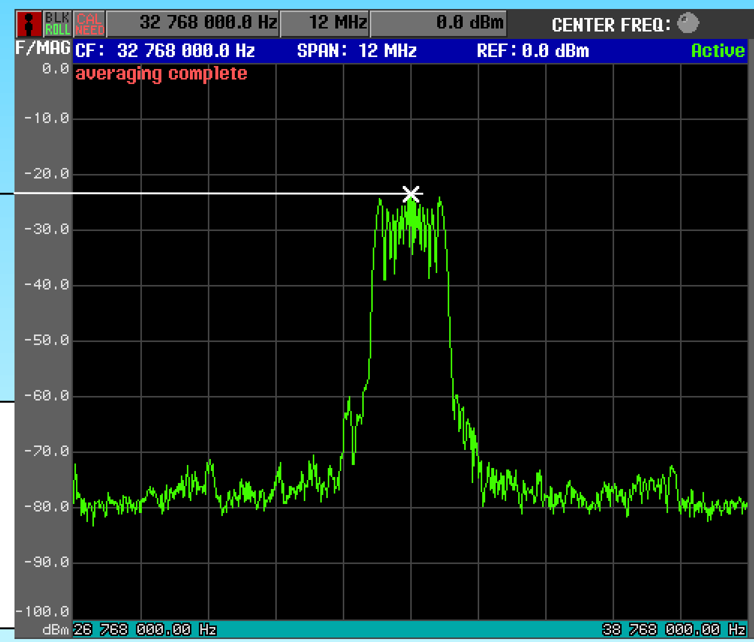
Spectrum Comparison from Spectrum Analyzer



-9.9 dB

-23.0 dB

-13.1 dBc EMI Reduction



SSC = No Spread

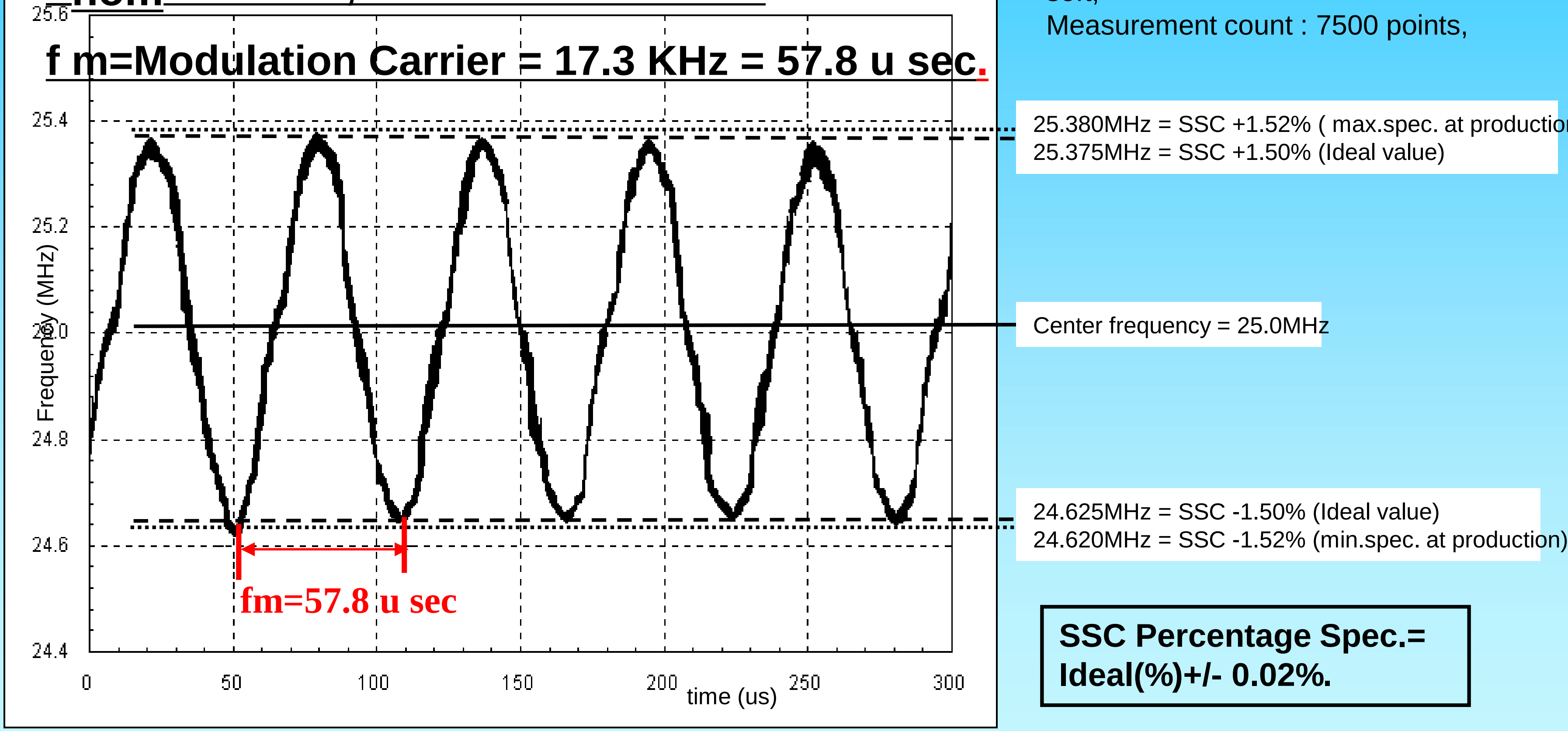
Center spread at ±1.5%

Modulation Tolerance is Well Controlled Under ±0.02%

VDD=3.3v,
Ta=Room Temp,
Oscilloscope: Tektronix TDS694C,
Probe : Tektronix P6245,
Data generator : Tektronix DG2030,
Frequency measurement : M1Jitter soft,
Measurement count : 7500 points,

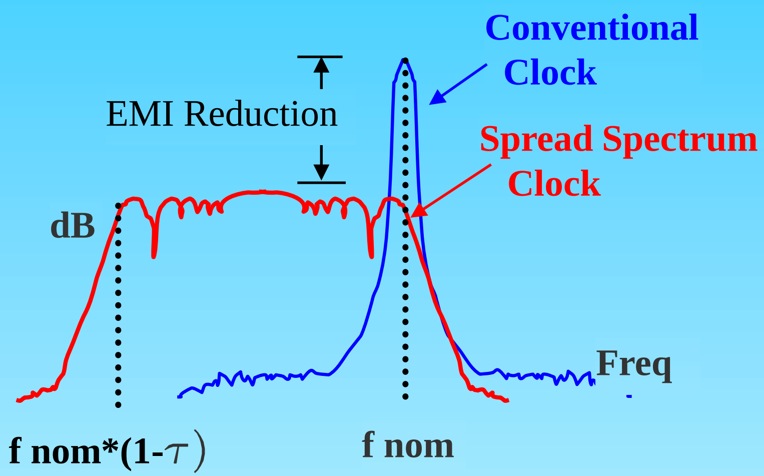
f nom = 25MHz; SSC = ±1.5%= C1.5

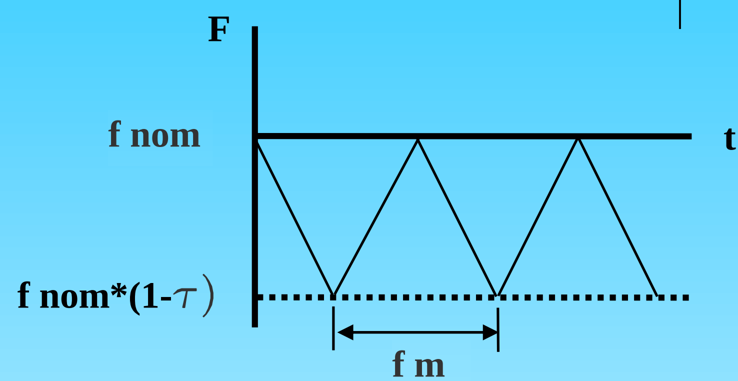
f m=Modulation Carrier = 17.3 KHz = 57.8 u sec.



SSC Percentage Spec.= Ideal(%)+/- 0.02%.

Type 2: Down Spread $f_{max} = f_{nominal}$

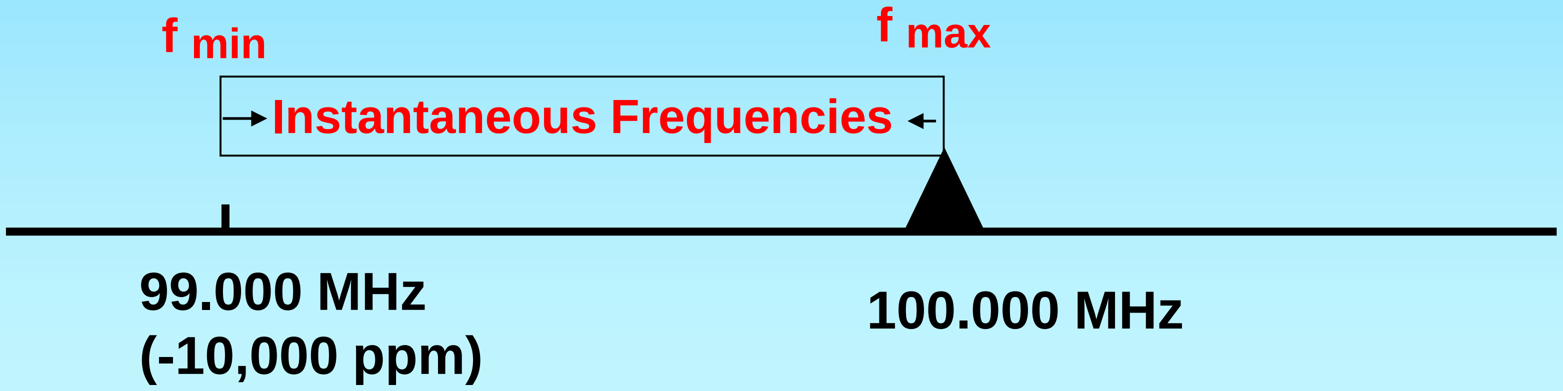




- $\Delta f_{up} = 0$; $\Delta f_{down} = \Delta f_{total}$
- Preferred spread type when over-clocking is a problem
- Drawback: Average system clock is slower

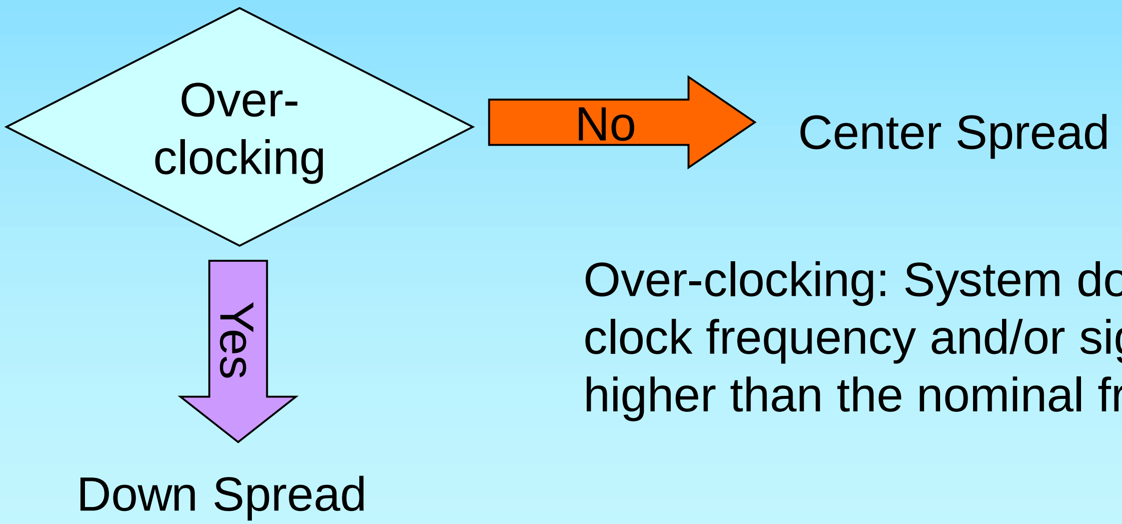
Example: 100 MHz with Down Spread 1% (-10,000 ppm)

Down Spread 1% (D1): Total Spread 1%



Characteristics of the Down Spread

- **Average system clock speed is slower than the non-Spread Spectrum Clock**
- **100% of the cycles is below the system clock.**
- **If don't know what spread type to choose: Try down spread first**



Over-clocking: System does not allow clock frequency and/or signal frequency higher than the nominal frequency

Instantaneous Frequencies between Frequency Boundaries (100 MHz as an example)

Total Spread %	Down Spread Instantaneous Frequency		Center Spread Instantaneous Frequency	
	min.	max.	min.	max.
	Down Range	Up Range	Down Range	Up Range
1 %	- 1%	0% 0 ppm 100.000000	-0.5 %	+0.5%
	-10,000 ppm		-5000 ppm	+5000 ppm
	99.000000		99.500000	100.500000
2 %	- 2.0%		-1.0 %	+1.0%
	-20,000 ppm		-10,000 ppm	+10,000 ppm
	98.000000		99.000000	101.000000
3 %	- 3.0%		-1.5 %	+1.5%
	-30,000 ppm		-15,000 ppm	+15,000 ppm
	97.000000		98.500000	101.500000

Group "R" vs Group "P"

	Group "R"	Group "P"
Frequency Range	3.5 ~ 160 MHz	13 MHz ~ 220 MHz
Modulation Carrier Freq.	6.9 KHz ~ 55.5 KHz	25.3 KHz ~ 58.6 KHz
Spread Percentage	Total 0.5%: C0.25; D0.5 (not available, if Tri-state chosen) Total 1%: C0.5; D1 Total 3%: C1.5; D3	Total 0.5%: C0.25; D0.5 Total 0.75%: C0.375; D0.75 Total 1.25%: C0.625; D1.25 Total 2%: C1; D2 Total 2.5%: C1.25; D2.5 Total 3%: C1.5; D3 Total 3.5%: C1.75; D3.5 Total 3.75%: C1.875; D3.75
Pin 1 option	Tri-state: Output high impedance when taken low.	Not Available
Jitter	±250 ps typical	±100 ps typical

EMI Reduction Applies to the whole Spectrum, not just one mode

In SST, once fundamental mode bandwidth is widened (spread, smeared), all harmonics get the same bandwidth x its harmonic number.

Example: 100 MHz with 1% total spread

- Fundamental mode: 1% of 100 MHz = 1 MHz band width
- Bandwidth of 3rd harmonic: 1% of 300 MHz= 3 MHz
- Bandwidth of 5th harmonic: 1% of 500 MHz= 5 MHz
- Bandwidth of 7th harmonic: 1% of 700 MHz= 7 MHz

Higher harmonic, higher band width, more EMI reduction

Design for Compliance

EMI Reduction you can calculate, you can expect, you can see.

$$\text{EMI Reduction (dB)} = 10 * \log_{10}[(\text{Spread}\,\%) * (\frac{\text{Fout in Hz}}{120\,KHz})]$$

- EMI reduction is determined by
  a. **Total spread %**
  b. **Output Frequency**
- Examples: Fout = 50 MHz, total spread is 2% (either center spread ±1% or down spread 2%):

At fundamental mode:

EMI reduction = 10x $\log_{10}$ (0.02x50E6/120E3) = 9.2 dB.

At 3rd harmonic:

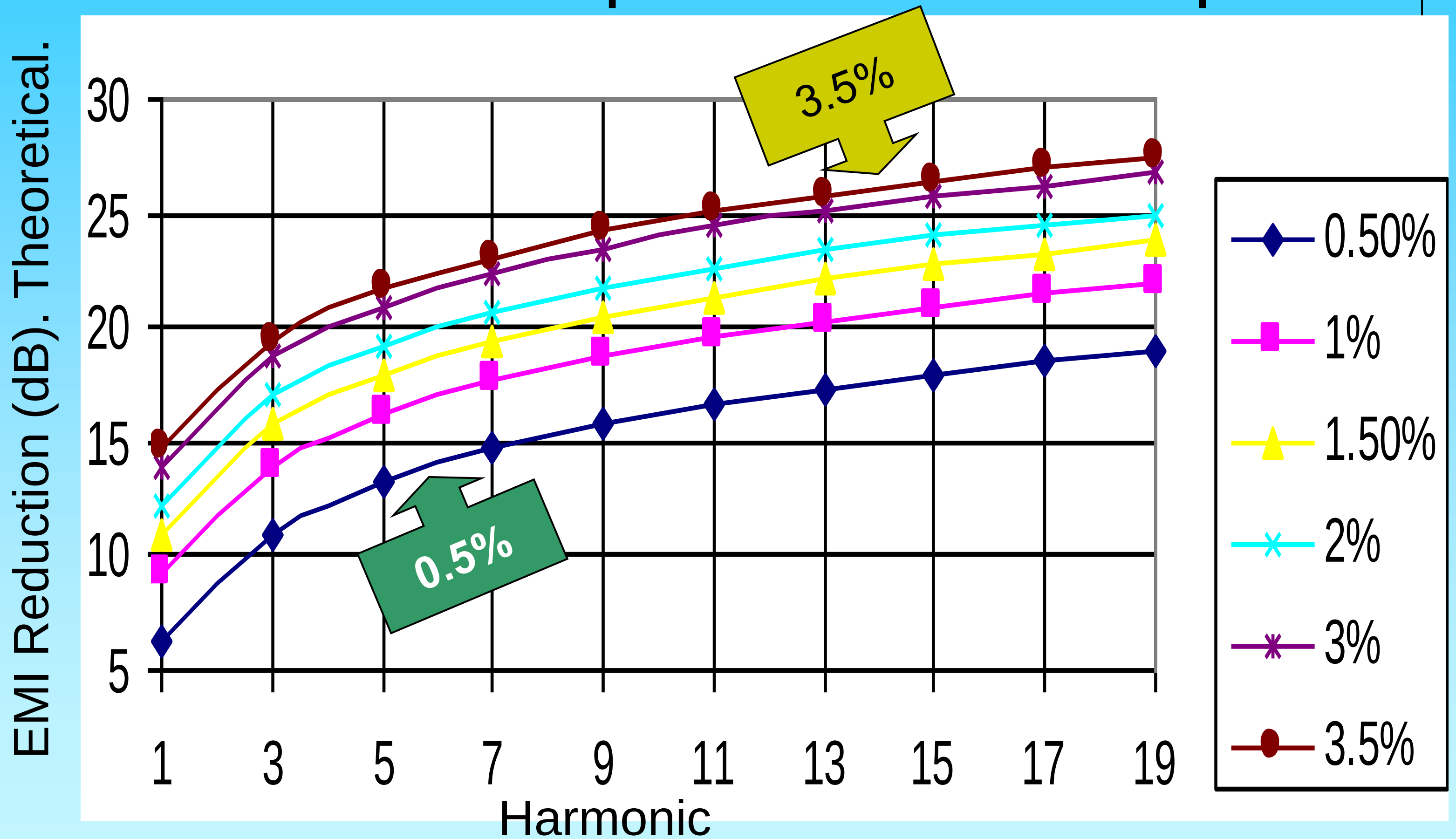
EMI reduction = 10x $\log_{10}$ (0.02x3x50E6/120E3) = 13.9 dB.

At 5th harmonic:

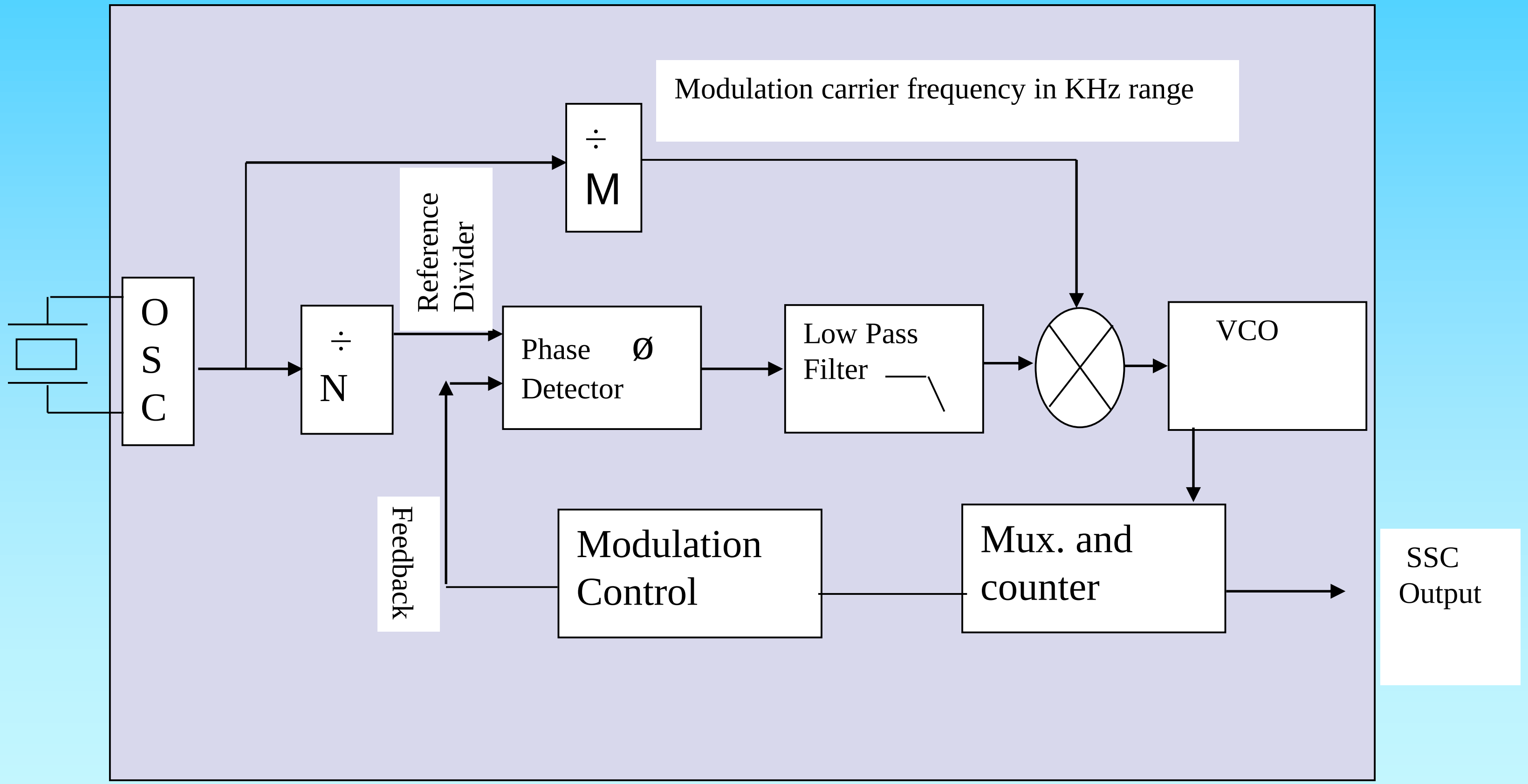
EMI reduction = 10x $\log_{10}$ (0.02x5x50E6/120E3) = 16.1 dB.

Pick Your Spread Percentage

Example: 100 MHz at various spread %



Spread Spectrum Clock Block Diagram



Negligible Impact on Jitter from SST: Low cycle-to-cycle Jitter

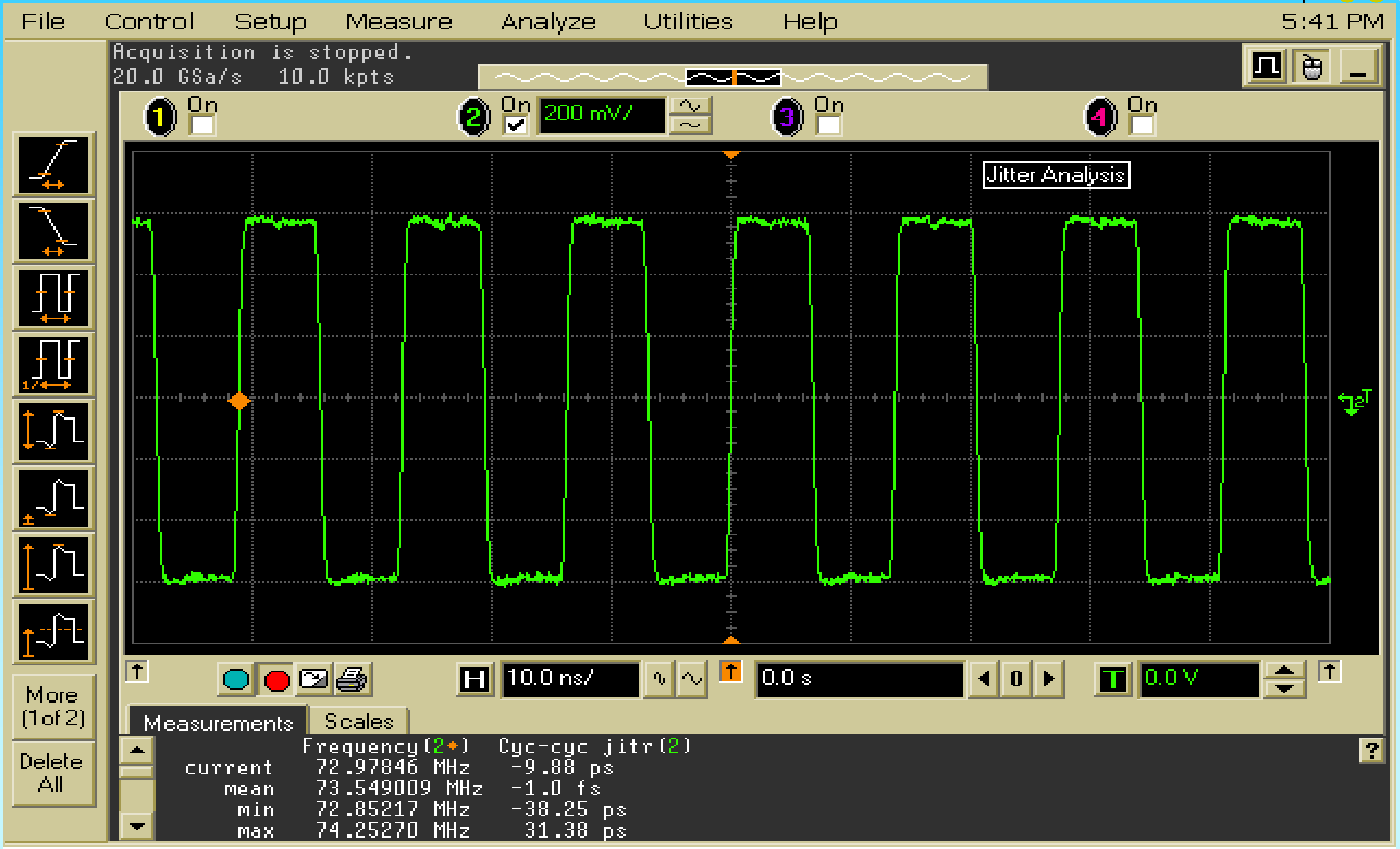
Continue the example of center spread ±0.5% (total 1%) from slide No. 11

- f nom.=100 MHz = 0.01u sec.=10n sec.
- f m = 34.688 KHz = 28.82 u sec.
- Cycle Ratio
  = Clock / Modulation
  = 2882 clock cycles / 1 modulation cycle

Cycle-to cycle Jitter contributed from SST modulation is < 0.05%

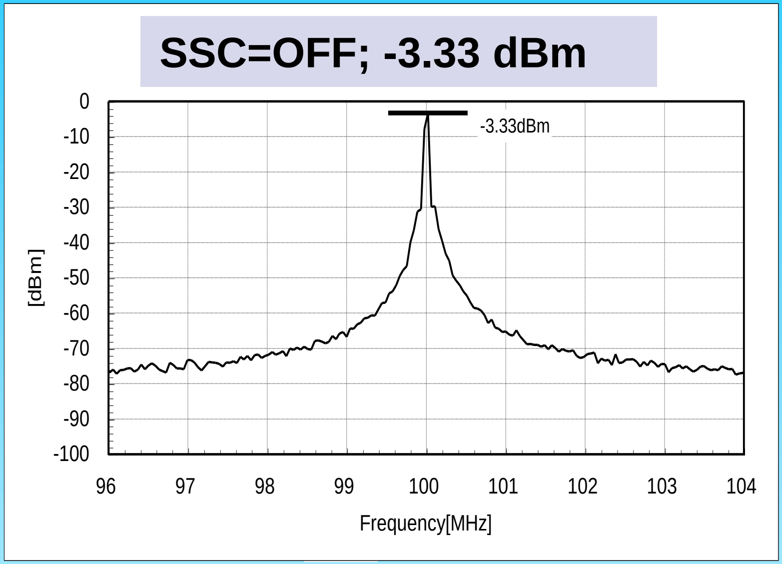
- 1% total change of 100 MHz =100 ps
- 100 ps/2882 cycles=0.034 ps per modulation cycle
- Due to background modulation, only cycle-to-cycle period jitter is specified.

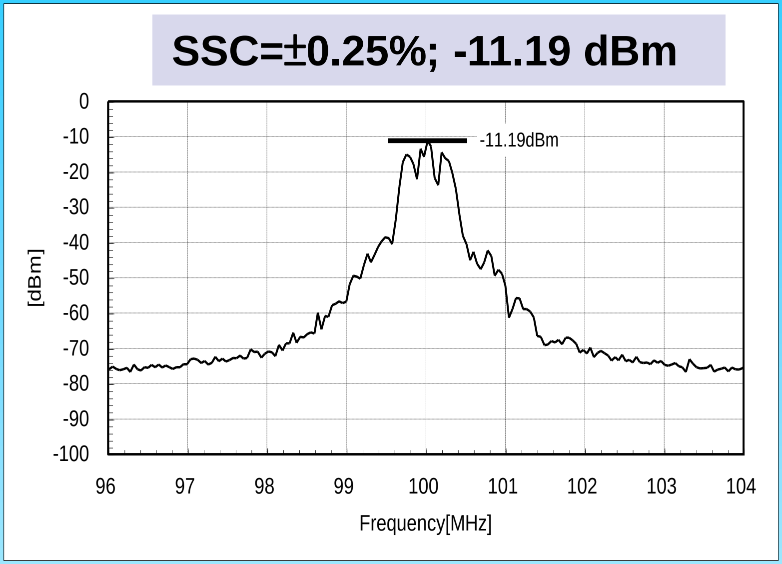
3HM57-25.000P Jitter

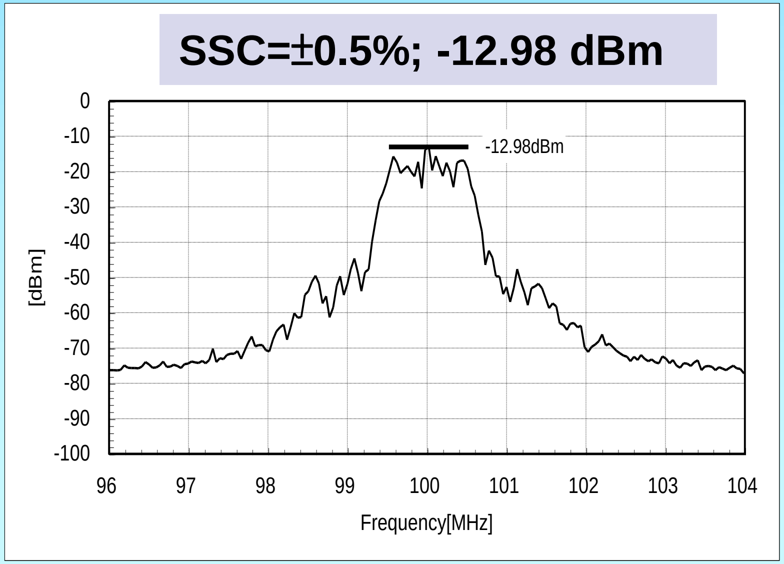


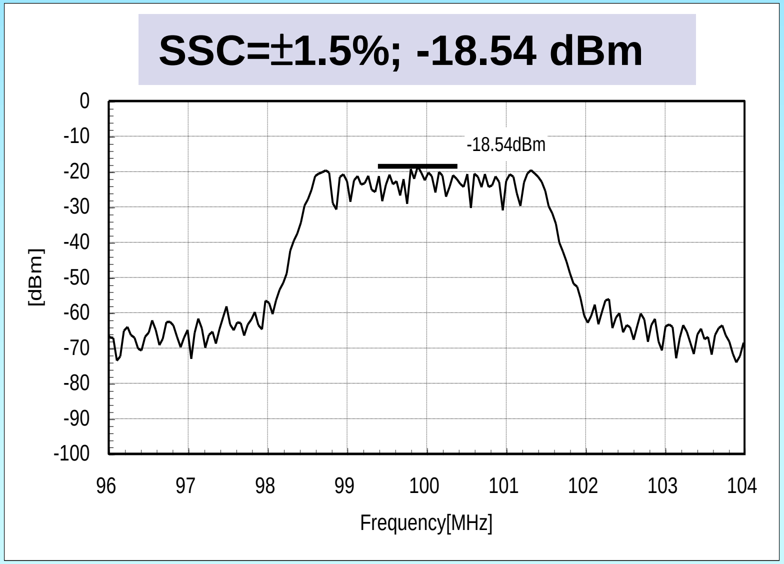
3HM57-B-100.000R at C0.25, C0.5 and C1.5 Spectrum Analyzer Waveform Data

VDD=3.3V, Ta=Room Temp.
Spectrum Analyzer : Tektronix 3026
Probe : Tektronix P6245



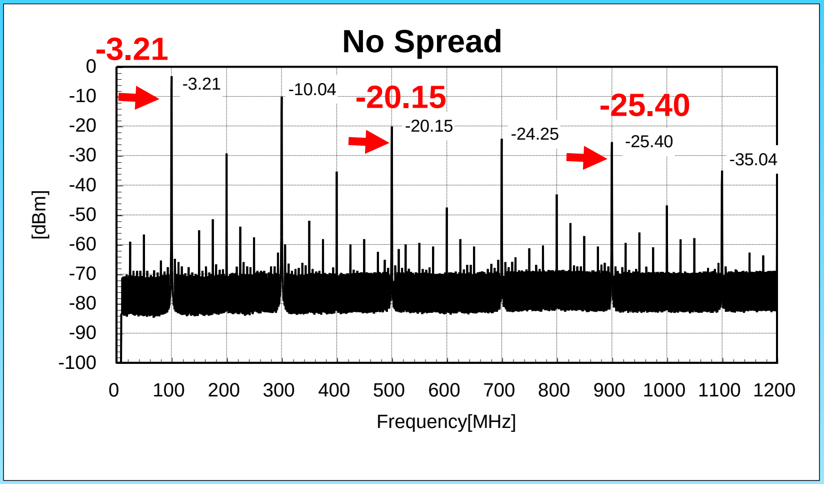


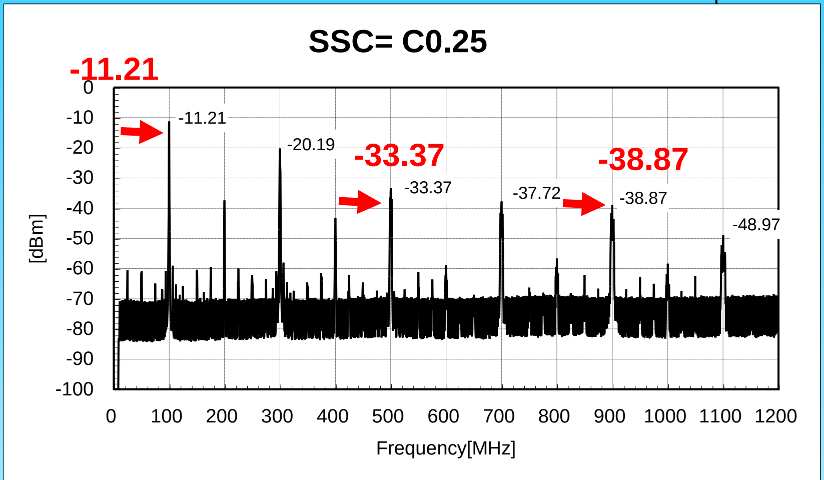


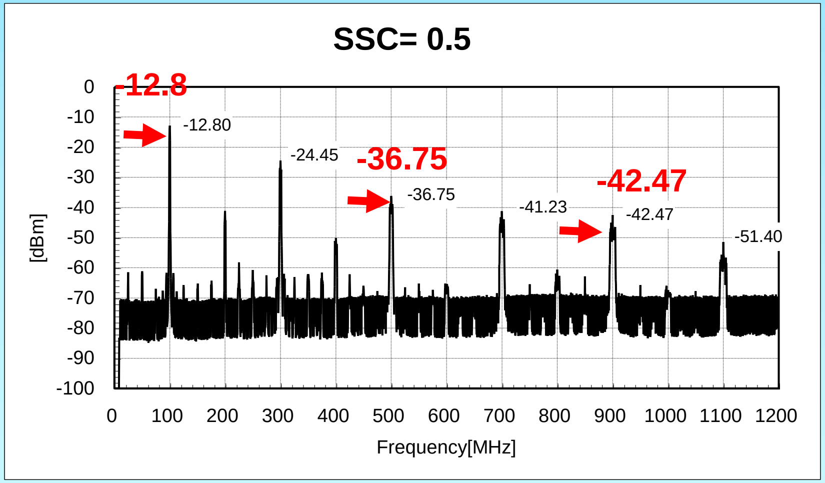


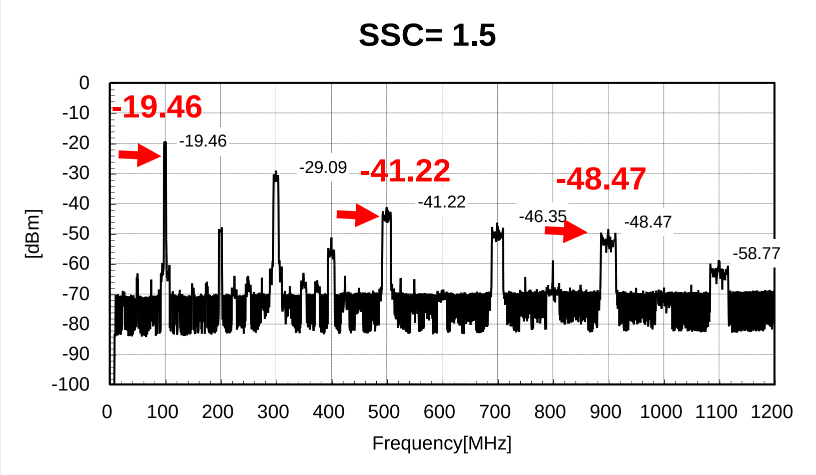
Spectra Comparison: 3HM57-B-100.000R at no spread, C0.25, C0.5 and C1.5

VDD=3.3V, Ta=Room Temp.
Spectrum Analyzer : Tektronix 3026
Probe : Tektronix P6245



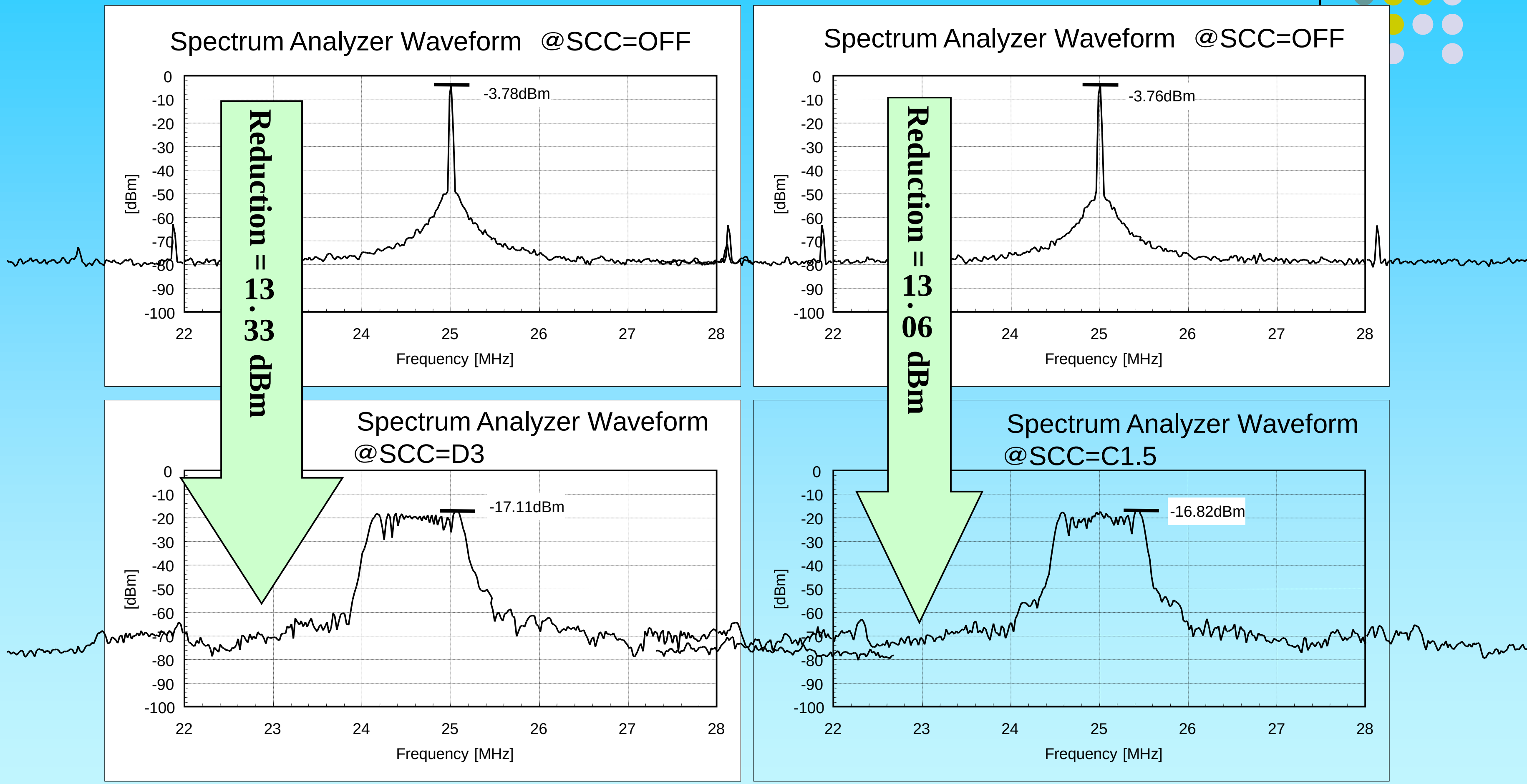




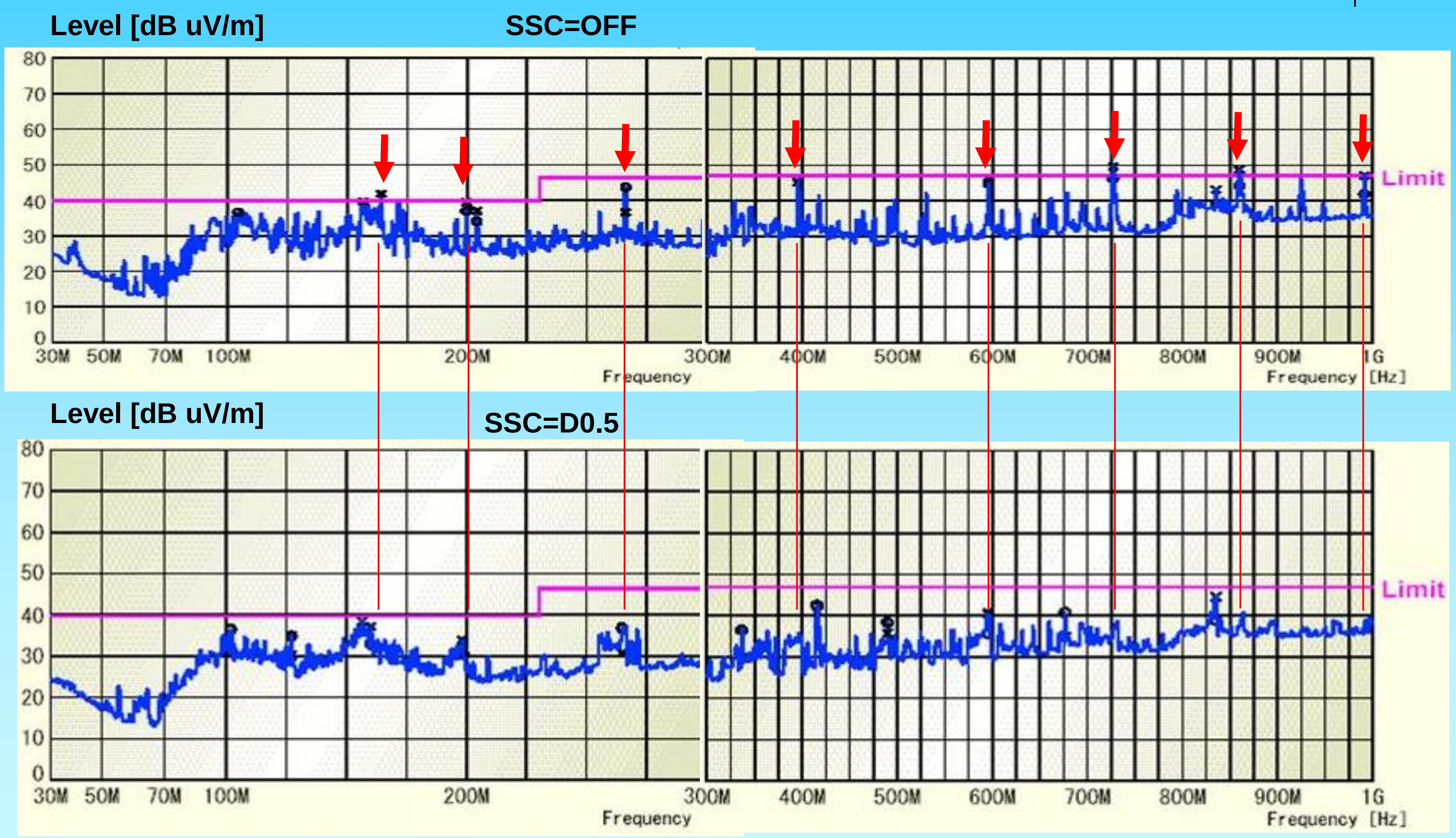


3HM57-100.0R at SSC=off, C1.5 and D3 (total 3%)   C1.5 ≈ D3

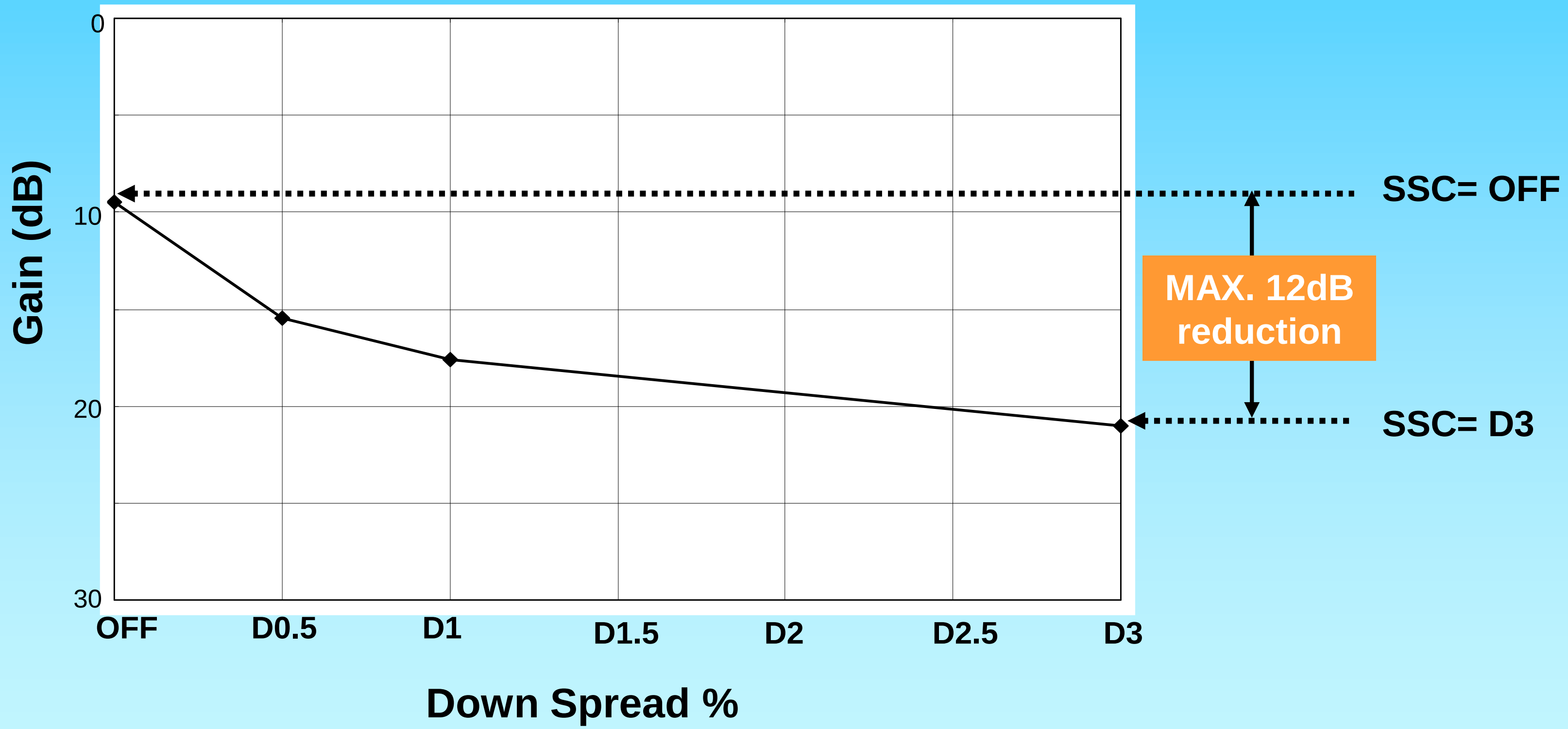
VDD=3.3V, fin=25MHz, Ta=Room Temp.
Spectrum Analyzer : Tektronix 3026
Probe : Tektronix P6245



Frequency Spectrum comparison – 3HM57-33.000-D0.5



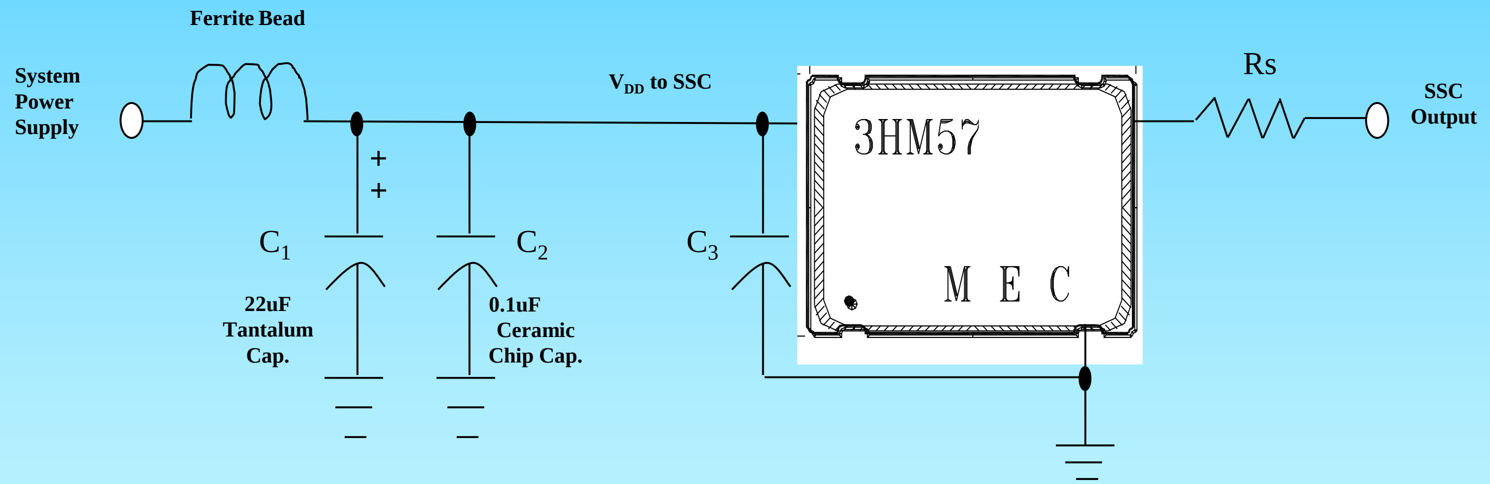
3HM57-48.000R at Various Down Spread %



- Ta=Room Temp
- Spectrum Analyzer : Tektronix 3026
- Probe : IWATSU SS-0012
- Data generator : Tektronix DG2030

Power Supply to the SSC

- ► Low Pass Π (pi) Filter
- ► Series Termination Resistor



Concerns of Using SSC

- Are down-stream PLLs able to track the dynamic frequency change from SSC?
- Is over-clocking a problem?
- What is right spread percentage for my application?
- Will the modulation carrier frequency resonates with other system clocks?
- When using center spread, make sure not to upset the system max. allowed speed

Traditional Ways to Deal with EMI / EMC Problems

• Metal Shielding, Gaskets	$4.0
• EMI Filtering (Ferrite beads, ferrite arrays, ferrite core, L-C combined chips, Common Mode Chokes and Toroids)	$3.0
• Multi-layer PCB	$3.0
• Trial-and-error engineering time	$80/hr
• Repeated EMI Testing time and fees	$1,000+
• Lost time-to-market	$ ∞

Main source of EMI: Conventional Clocks

Solution from Mercury: Spread Spectrum Clocks <$1.0

Benefits of using Mercury Spread Spectrum Clocks - 1

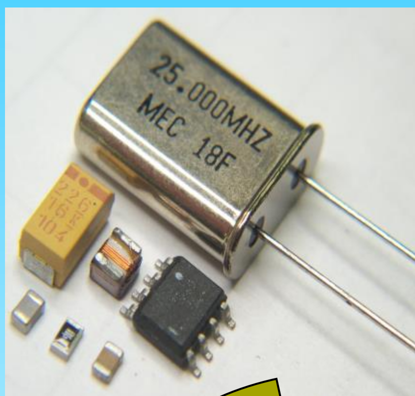
- 7+ dB EMI reduction. 20+ dB on higher order harmonics.
- Reduce EMI at its source – The clock
- EMI reduction applies to the fundamental frequency and all harmonics.
- Drop-in Replacement for your existing clocks

  (Packages are available from 5x3.2, 5x7 to full size 4 pin DIP)

Benefits of using Mercury Spread Spectrum Clocks - 2

- **Compact, miniature, reliable, space-saving solution**
- **Whole package is grounded**
- **Reduced board level parasitics**
- **Controlled loop length and matched impedance**
- **Integrated load capacitance to improve oscillation start-up**
- **Integrated Loop filter built-in**
- **Integrated power supply filtering (an option)**
- **EMI suppression for all harmonics**
- **Deal with the EMI problem during design stage**
- **Benefit every harmonic. The higher the harmonics, the more EMI reduction.**
- **Faster time-to-market**

Spread Spectrum Clock Oscillators



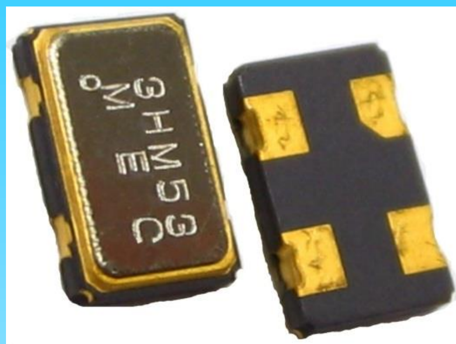
► **Discrete Type: Spread Spectrum IC + external crystal +loop filter + power filtering + impedance matching**

► **Integrated Type: Mercury HM series Low EMI oscillators**

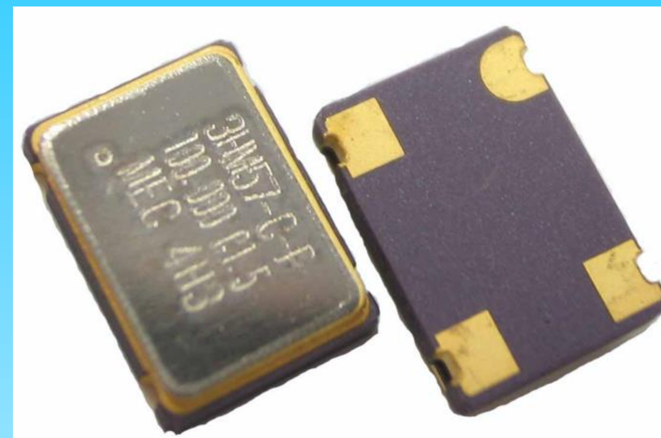
Low cost

Design for Compliance

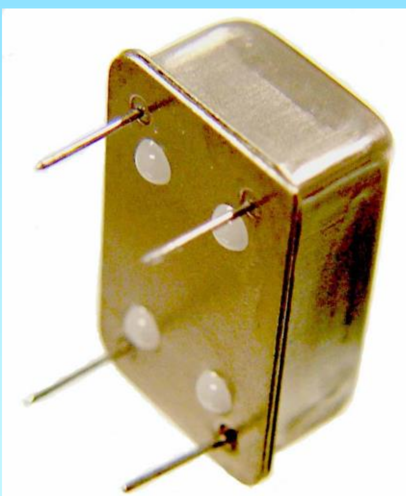
HM Series Packages



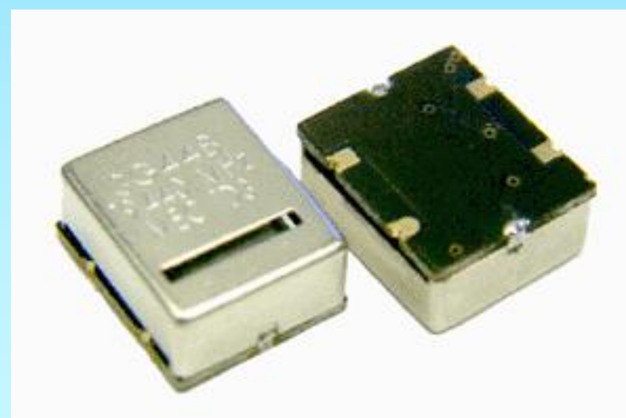
HM53: 5x3.2x1.2 mm



HM57: 5x7x1.8 mm



HM14: Full size 4 pin DIP



HM44: 9.6x11.4x4.7 mm

Application 1: Oak OTI-4110 (Programmable System-on-a-Chip)

- Product: HP L1500 color laser-Jet printer
- To pass FCC class B Regulations.
  Clock Frequency: 48.000 MHz. USB 2.0 PHY

- Mercury Solution: 3HM57-BT-48.000R-C0.5
  Group R, Center Spread 0.5%, carrier 16.650 KHz

  Instantaneous Freq. min.:
  47.760 MHz (-0.5%, -5,000 ppm)

  Instantaneous Freq. max.:
  48.240 MHz (+0.5%, +5000 ppm)

Application 2:
Intel IXP420 Network Processor
Intel IXC1100 Control Plane Processor

- Internal system clocks and external interface clocks: All referenced to an external reference clock through PLL

- Intel spec.: To pass FCC class B Regulations.
  Clock Frequency: 33.33 MHz ± 50 ppm.
  Deviation: -2% min.; 0% max.
  Modulation Frequency: 50 KHz max.
  No over clocking

- Mercury Solution: 3HM57-BT-33.330R-D1
  Group R, Down Spread 1%, carrier 23.123 KHz
  Instantaneous Freq. min.: 32.996700 MHz (-1%, -10,000 ppm)
  Instantaneous Freq. max.: 33.330000 MHz (0%, 0 ppm)

Application 3:
Sigma Designs EM8620 Media Processor

- Products: LG's LCD-TV; D-Link's Networked Media Player; Pioneer's 50" plasma display; Buffalo's LinkTheater DVD media players; IO Data's AVel Link players; IPTV set top boxes
- To pass FCC class B Regulations.
  Clock Frequency: 27.000 MHz.
  Carrier: 31.5 KHz max.

- Mercury Solution: 3HM57-BT-27.000R-C0.5
  Group R, Center Spread 1.5%, carrier 18.731 KHz

Instantaneous Freq. min.:
26.865 MHz (-0.5%, -5,000 ppm)

Instantaneous Freq. max.:
27.135 MHz (+0.5%, +5000 ppm)

Successful Applications of Mercury Spread Spectrum Clocks

- Medical
- Printers (ink jet, laser beam)
- LCD Flat Panel Displays
- Digital Cameras
- Surveillance Cameras
- Networks
- Wireless LANs, WANs
- Automotive
- Copy Machines
- CPUs that takes SSC
- PDAs
- Scanners
- CD-ROM, VCD, DVD
- GPS Car Navigators
- Cellular phones with built-in color LCD and digital camera